UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,707	11/21/2001	Woong Lim Choi	K-0346	9583

34610 7590 09/09/2003

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER
DINH, SON T

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/989,707	Applicant(s) CHOI, WOONG LIM	
	Examin r son t dinh	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-66* is/are allowed.

6)☒ Claim(s) *1,2,4-13,67 and 68* is/are rejected.

7)☒ Claim(s) *3,69-73,75 and 76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history* .

DETAILED ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-9, 13, 67 are rejected under 35 U.S.C. 102(e) as being anticipated by Harari et al (U.S. Pat No 6,151,248).

With respect to claims 1 and 67, Harari et al(see figures 4 and 5) disclose a non-volatile memory device comprising a semiconductor substrate (45,fig 4) having active (49, 51, fig.4) and field (L-1, L-2, fig.4) regions, at least two non-volatile storage transistors (55, 56, 81, 57, 58,83, figure 5: or 57, 58, 51 in figure 4) each having the active region (49, 51, figure 4) and a control gate (83, figure 4 and 5), wherein the control gate 83 is incorporated in a single control plate, at least two selection transistors (T2, and another connected to the right side of floating gate transistor 51, 83, 58, not shown in figure 5), wherein each of the selection transistor (T2) is connected to the corresponding non-volatile transistors.

With respect to claim 2, column 9, lines 10-15 clearly teaches that the semiconductor substrate 45 is a triple well type having an N-type well on a P-type substrate and a P-type well in the N-well, wherein each active region 49 and 51 (see figure 4) is formed on the P-type well.

With respect to claim 4, since the selection transistor (99, 49, 51, figure 4) shares a common channel of the non-volatile transistor, then both transistors are connected in series through a common channel.

Regarding claim 5, column 8, lines 64-68, and column 9, lines 1-9, discloses that there are a plurality of dielectric layers (the dielectric between 99 and 103 and 105 in figure 4) which have different thickness.

With respect to claims 6 and 9, the storage elements 57 and 58 in figure 4 are conductive floating gates.

With respect to claim 7, the dielectric layers (the layers between 99 and 103, figure 4) are formed of tunneling oxide (see column 8, lines 55-63).

With respect to claim 8, the dielectric between 103 and substrate 45 (figure 4) would be a first dielectric layer, and the dielectric layer between 99 and substrate 45 (figure 4) would be a second dielectric layer.

With respect to claim 13, the two non-volatile transistors (58, 83, 57, figure 4) have at least one common impurity region (51) for source and drain in the substrate 45.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-12, 68 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al in view of Essaian (U.S. Patent No 5,877,977).

Harari et al applied as above. Also, the control gate 83 and storage gate 57 and 58 in figure 4 of Harari et al are formed in a split gate structure as claimed in claim 74. The only difference between Harari et al and claims 10-12, 68 and 74 is that Harari et al fail to teach a storage which is made of nitride (as claimed in claim 10) and ferroelectric (as claimed in claim 12). Essaian discloses a non-volatile memory cell comprising a storage that is made of nitride and ferroelectric material (see column 2, lines 50-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Harari et al by using a nitride layer and a ferroelectric material to form a storage for storing data as taught by Essaian.

Allowable Subject Matter

Claims 3 and 69-73, 75-76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 14-66 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to disclose a memory device comprising a two non-volatile storage transistor that share a common (or single) control gate combined with a selection transistor that is connected in series with the non-volatile storage transistor

through a PN junction shared by the selection and non-volatile storage transistor (as claimed in claim3), or each selection transistor including a source and a drain in the substrate, a selection gate on the dielectric on a dielectric layer, wherein the source of each of the selection transistor acts as drain of the corresponding non-volatile storage transistor (as claimed in claims 14, 18 ,26, 34, 36, 41, 45, 47, 48, 50, 54); a memory device having a first transistor with a control gate and a storage gate and a second transistor having a selection gate, wherein the first transistor of each cell includes first and second electrodes and the second transistor of each cell includes a first and second electrodes, the second electrode of the first transistor is commonly coupled to the first electrode of the second transistor (as claimed in claims 69, 73 and 75).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ***.

-Wong disclose a memory device having a common floating gate.

-Nakagawa et al disclose a memory device having storage gate.

-Arima et al disclose a memory device including a control gate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Dinh whose telephone number is 703-308-4120. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 703-308-2816. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

S. Dinh
August 29, 2003

Son T. Dinh
Primary Examiner

T